...We *are* boundary-scan.

JTAG TECHNOLOGIES®

WWW.JTAG.COM

datasheet *Pro*Vision

Easiest, fastest toolsuite for development of test and ISP applications

Unmatched flexibility: multiple chains, multi-board designs, re-usable project database

Integrated fault coverage analysis, application sequencing, and graphical viewing and control

...We *are* boundary-scan.

Professional / Visual Boundary-Scan Development System

Overview

JTAG Technologies offers a comprehensive line of hardware and software products to test and program printed circuit boards in compliance with the IEEE 1149.1 and related boundary-scan standards. The IEEE specification defines a 4- or 5-wire electrical interface and control protocol to communicate with the target board, providing superior access to complex, high-density PCBs.

ProVision™ is the all-in-one, professional grade development system for preparation of all boundary-scan test and in-system programming applications. The tool is highly automated, taking maximum advantage of a library of thousands of device models to rapidly generate tests and programming routines. All applications can be optimized, validated, and run within the ProVision environment prior to delivery of finished sequences to the manufacturing/testing facility.

ProVision's development features are tightly integrated with JTAG Technologies' advanced test coverage analysis tool and with JTAG Visualizer™. Working together, these tools enable the engineer to rapidly grasp the thoroughness of the test under development and to make improvements prior to release.

Features

- Easy-to-learn, easy-to-use graphical platform for rapid preparation of all boundary-scan test and in-system programming applications
- Highly automated development toolsuite handles non-boundary-scan devices via extensive model library
- Automatic generation of tests and diagnostics for advanced digital networks based on IEEE 1149.6
- Integrated testability analysis of maximum theoretical fault coverage and actual achieved level
- Integration with JTAG Visualizer for graphical viewing and control of nets and devices
- Built-in sequencer to prepare factory-ready boundary-scan test and ISP routines
- Multi-chain, multi-board support without complex netlist merging
- Compatible with all JTAG Technologies production software and controllers
- Import function for applications developed with previous generation of JTAG Technologies tools

JTAG ProVision Applications

Boundary-scan testing

- Board-level, system-level and board-to-board testing
- Full set of 1149.1 and 1149.6 tests and diagnosis: infrastructure, interconnection, clusters and advanced digital networks such as high-speed LVDS and ac-coupled networks

Flash programming

- Enhanced Throughput Technology™ with AutoWrite™, Ready/Busy, and VPP support
- Full functionality including blankcheck, read-ID, erase, program and verify for NAND and NOR flash devices

PLD programming

- Support for all industry formats, SVF, JEDEC, JAM, STAPL, IEEE 1532
- Universal and concurrent programming of CPLDs from multiple vendors

Full Automation

- Automatic recognition of boundary-scan chain topologies
- Automatic recognition of IEEE 1149.1, IEEE 1149.6 and non-scan device types
- Automatic safe setting of components as needed for the application
- Automatic board settings (guarding values) based on component models
- Flexibility to manually override settings at component and net levels

Next Generation, Project-Oriented Tool Suite for Developers

JTAG ProVision, the Professional/Visual development system from JTAG Technologies, delivers the ultimate in ease of use while meeting your need for a high-performance, high-quality development tool. Because it requires minimal boundary-scan knowledge and little design detail, ProVision enables you to generate applications quickly, focusing on optimizing the testability of your designs. Boundary-scan topology is analyzed automatically, even for complex multi-chain arrangements. Models for thousands of different non-boundary-scan devices allow JTAG ProVision to automatically control signals on your board for optimum test coverage and ISP performance while providing safe conditions on all board components.

JTAG ProVision's project-orientation supports multiple levels of system complexity, from single-board to multi-board designs. The tool's flexibility enables it to meet the needs of companies of all sizes, from those handling a few prototypes each year to large enterprises with many ongoing projects. Applications can be archived for porting between development platforms or to any runtime environment including to a contracted manufacturing location for prototyping, production, and repair.

The design wizard guides you intuitively with almost no learning curve, requiring minimal knowledge of the boundary-scan protocol. Although JTAG ProVision handles even complex designs reliably and thoroughly, it is easy to:

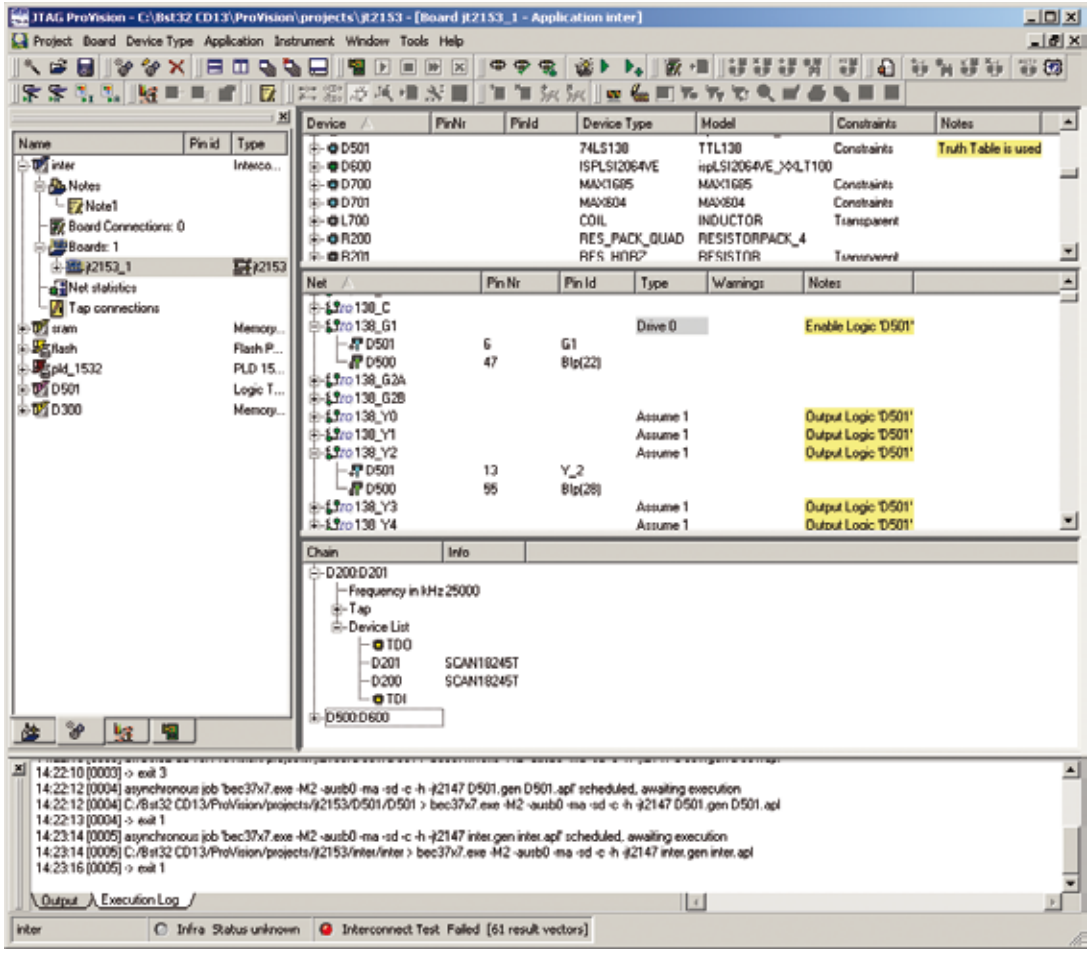
- **Create boundary-scan applications directly from the design engineering CAD data**
- **Analyze testability of your design and obtain theoretical and actual test coverage results**
- **Modify boundary-scan applications in case of a design re-spin**
- **Re-use boundary-scan and non-boundary-scan information for a new project**
- **Transfer applications to other production sites, both OEM and contracted**
- **Develop runtime-ready test sequences**

Managing Your Design

The foundation of JTAG ProVision is the project database, consisting of the relevant design information (netlists, BSDL files and models for non-boundary-scan devices) required for your boundary-scan applications. Built-in utilities allow you to explore and manage the project database, view the results, and generate boundary-scan applications.

Netlists

Netlists, imported from the board design environment, describe the connectivity of your board or system and the device types contained within the design. JTAG ProVision imports this information from your CAD system. The Bill of Materials can also be imported, an important feature if you wish to specify parts not placed on specified versions of your board.



Development screen with Device, Net, and Chain views

Powerful Benefits of JTAG ProVision

- Requires only minimal knowledge of boundary-scan and the design
- Rapid application development time, and no test language to learn
- Integration with JTAG Visualizer provides graphical interaction with design
- Support for multiple users and projects with a single, unified device data base
- Handles single and multiple board designs

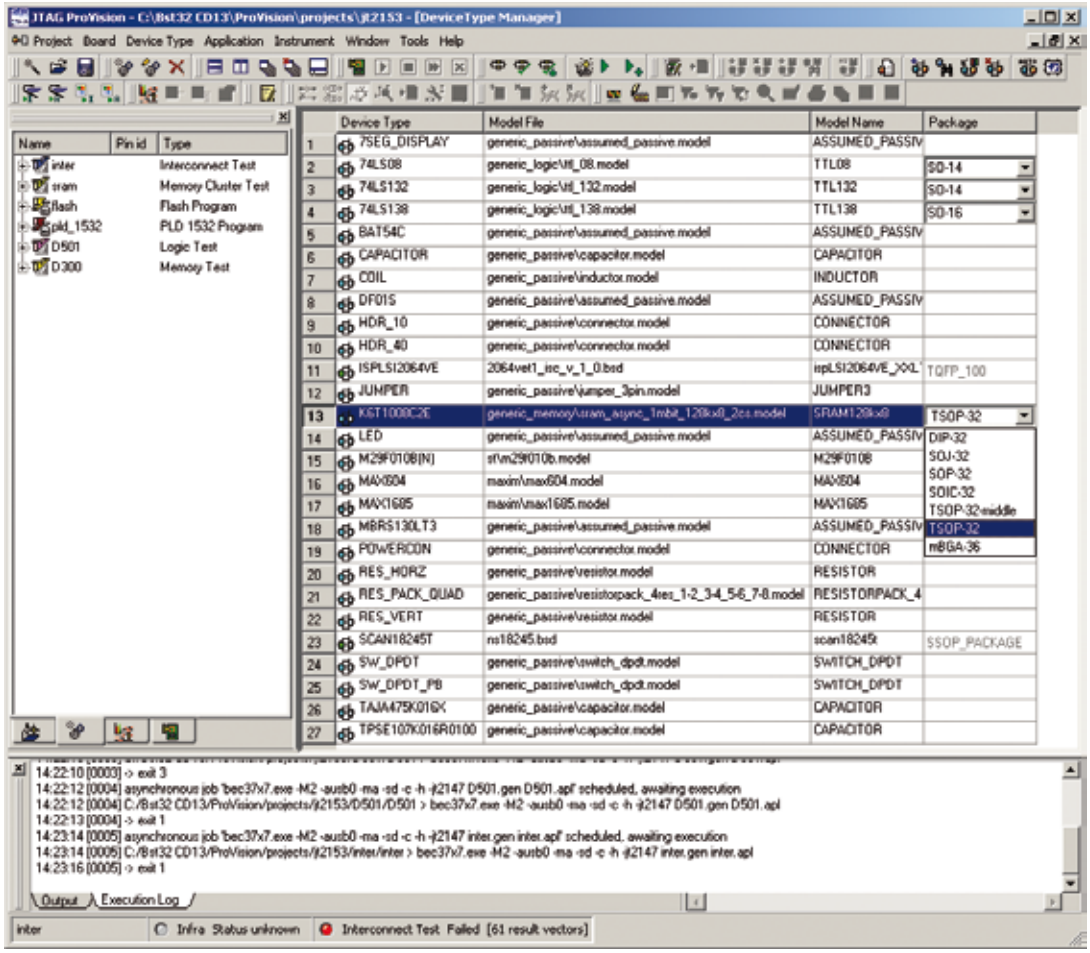
BSDL files and Device Models

IEEE 1149.1, 1149.6 and 1532 BSDL files describe the topology and function of the boundary-scan components in your design. When a new device is added to the project database, the corresponding BSDL file from the device manufacturer is automatically checked for syntactic accuracy.

JTAG ProVision includes an extensive library of models for non-boundary-scan devices and flash memories. Models provide control information for automatic enabling and disabling to ensure safe testing and in-system programming. The flash library supports automatic generation of boundary-scan applications for in-system flash programming. The device library is expanded regularly with over 4,650 device families now included, covering more than 28,500 devices.

Device Type Manager

Device types contained in the netlists are associated with BSDL files and models in the component library. New designs are incorporated quickly into the project data base by referencing existing device types to component models. JTAG ProVision's mapping structure supports diverse communities of users, such as a contract manufacturer with multiple clients.



Device type manager shows the relation of device types with BSDLs and models

Process Flow with JTAG ProVision and JTAG Visualizer

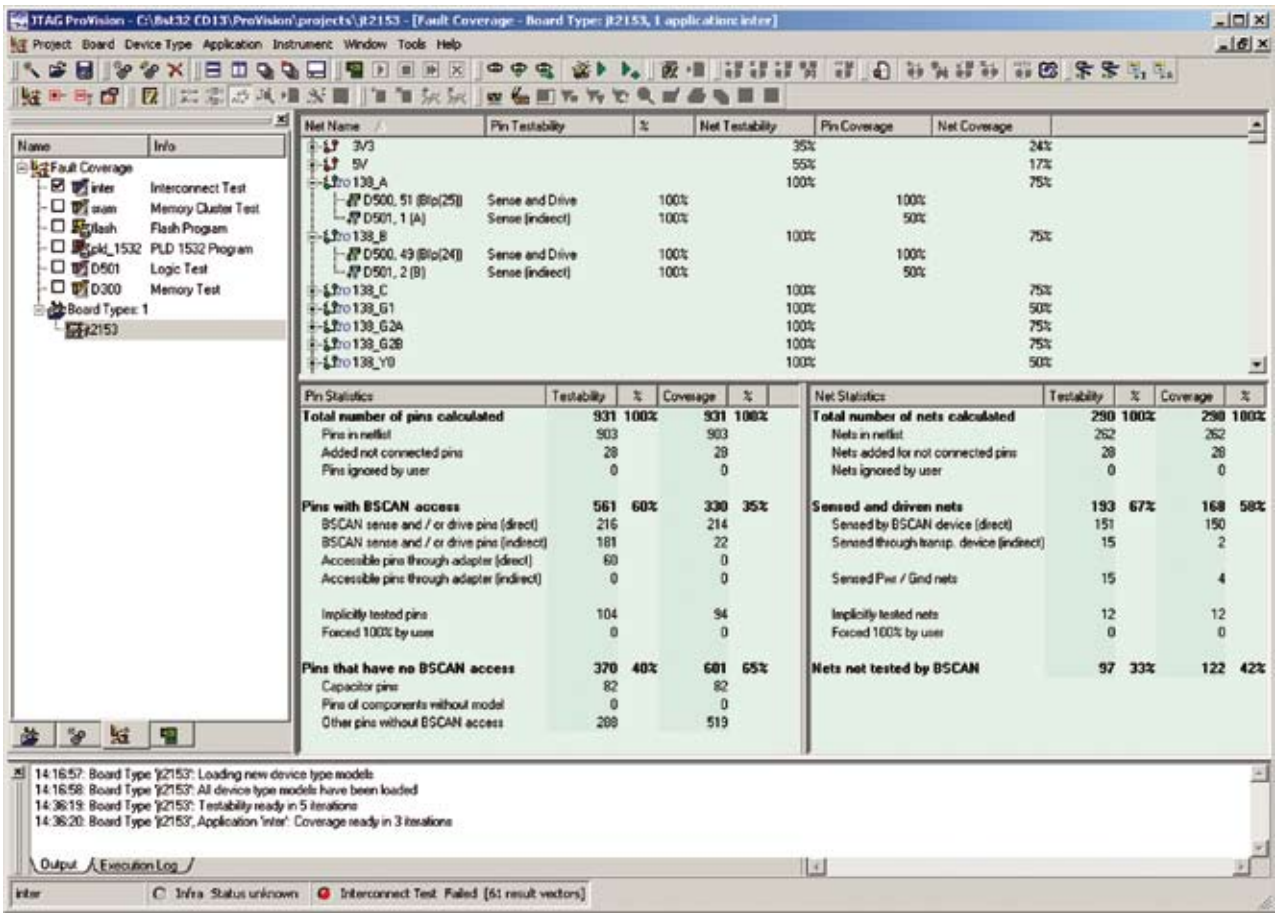
JTAG ProVision's wizard guides the development process using the same graphical interface for your tests and programming applications. As your design proceeds, the Resources tab of the development screen shows all of the pertinent information and gives you easy access to the underlying details. The Applications tab provides an index of the various tests and programming routines as they are developed. ProVision helps you generate a full set of tests--boundary-scan infrastructure, interconnects, memory testing including buffer and multiplexer support, clusters, and dot6--all automatically. The Fault Coverage tab brings up the theoretical testability that is achievable for your design as well as the actual coverage as the tests are generated. The fourth tab, Sequencing, allows you to create sequences of your tests and programming applications as they will be executed in the production environment. JTAG ProVision sets control signals (enable, disable, transparent, etc.) automatically, as required to optimize test coverage. If your design includes IEEE 1149.6- compliant devices (such as high-speed SER-DES parts), the appropriate interconnection tests are developed automatically. NetExplorer shows you the settings made

by the tool based on the device models. If desired, automatic settings can be overridden manually for the high degree of flexibility and control demanded by experienced test engineers.
ProVision is integrated with JTAG Visualizer providing two-way interaction to your design. You can see graphically where a specific net appears in your schematic and layout. Visualizer allows you to flip and rotate the board, allowing you to "see" it in different orientations, flipping it over to see the bottom or rotating it for clarity. Furthermore, Visualizer gives you direct graphical control of your design, allowing you to set constraint values on nets and devices. Another power Visualizer feature is Worldview, in which a small window indicates which part of the board or schematic is being displayed. You can move the window to view a different portion of the board or schematic.

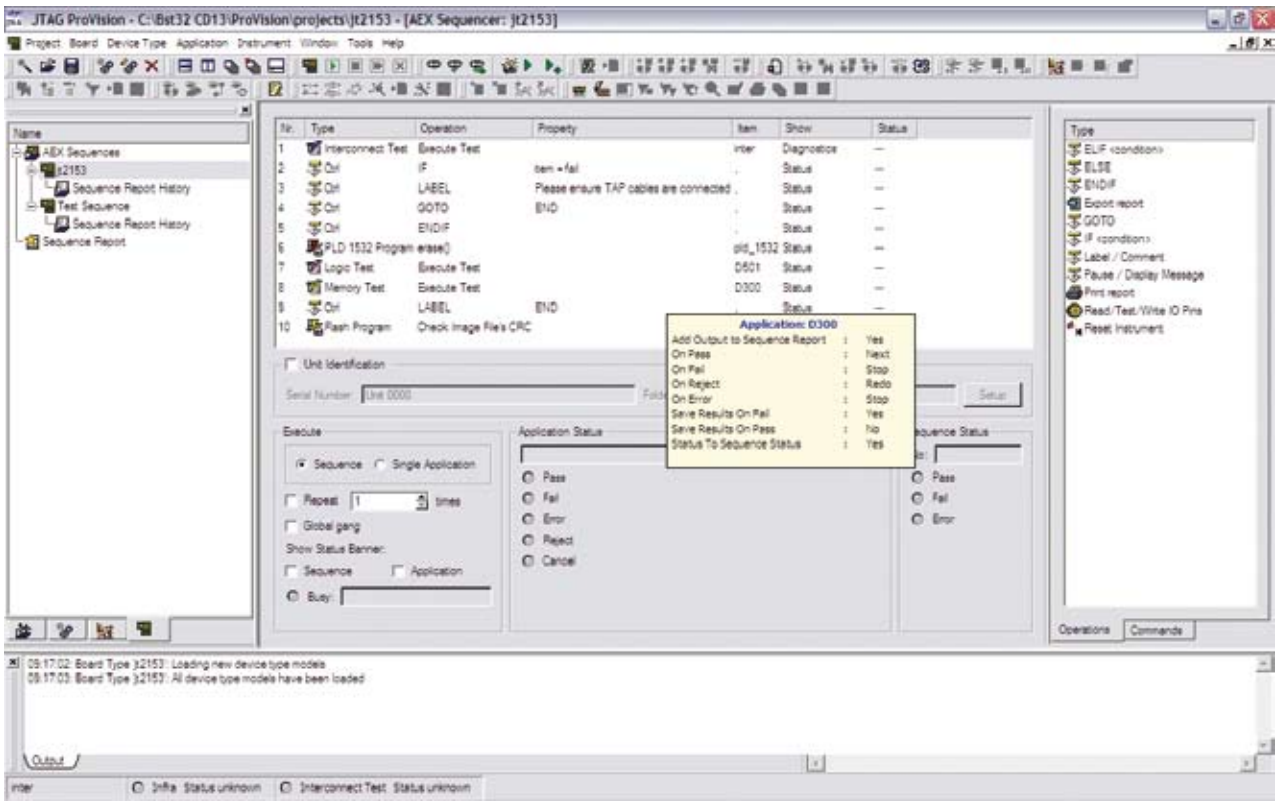
Test results are provided in a highly informative truth table, with net details available by simply "hovering" the mouse. Diagnostics interpret the results and indicate the probable failure cause(s), down to the pin level in most cases, even for IEEE 1149.6 test failures.

You can easily generate system-level applications by means of JTAG ProVision's Connection Editor. This facility supports graphical definition and editing of connections between the target board and other target boards or DIOS modules.

All tests and ISP applications are immediately available for validation within JTAG ProVision. Archiving of applications facilitates porting to other development platforms and to your production environment. For production purposes, use ProVision's built-in sequencing capability to prepare factory-ready boundary-scan test plans with conditional branching, flow control and user commands. Multi-level password control provides security for modifying and executing sequences. Alternatively, other executive programs such as National Instruments' TestStand create the sequence and execute the applications. By means of the many integration solutions offered by JTAG Technologies, applications can be incorporated easily within your in-circuit test systems, flying probers, and functional test systems.



Fault Coverage tab shows test coverage for your design



ProVision allows you to create test and ISP production sequences

JTAG ProVision Architectural Highlights

- Unified GUI for all applications
- Wizard guides the development process
- Device library supports multiple projects with common data base
- Automated development via advanced generation tools (for test, flash, and PLD) in conjunction with the device library
- Analyzes theoretical and actual fault coverage
- Links to JTAG Visualizer for graphical view and control of nets and devices
- Faults are reported with full diagnostics and truth-table detail, including support for IEEE 1149.6
- Archiving of applications for convenient porting to other development or production systems
- Built-in sequencer to prepare factory-ready test plans

Ordering Information

Ordering Name	Platform Description
ProV_PL / T / *	Execution and compilation platform licensed for test
ProV_PL / F / *	Execution and compilation platform licensed for flash
ProV_PL / P / *	Execution and compilation platform licensed for PLD
ProV_PL / A / *	Execution and compilation platform licensed for ALL: test, flash, and PLD

* = PL License Type: L for LAN, N for node-locked

Ordering Name	Generator Description
ProV_GT / T / **	Test generators for interconnection, memory and cluster tests with fault coverage
ProV_GT / F / **	Flash programming generation and library (NOR & NAND flash, serial EPROMs)
ProV_GT / P / **	PLD programming generators including support options for IEEE 1532, JEDEC, JAM, STAPL, SVF
ProV_GT / A / **	Generators for ALL: test, flash, and PLD

** = GT License Type: W for WAN, L for LAN, N for node-locked

...We *are* boundary-scan.

JTAG TECHNOLOGIES®

WWW.JTAG.COM

USA, Canada and Mexico
Phone: (Toll Free) 877 FOR JTAG
Fax: 410 604 2109
Email: info@jtag.com

Germany
Phone: +49 (0) 971 699 1064
Fax: +49 (0) 971 699 1192
Email: germany@jtag.com

Europe and rest of the world
Phone: +31 (0) 40 2950870
Fax: +31 (0) 40 2468471
Email: info@jtag.nl

United Kingdom & Ireland
Phone: +44 (0) 1234 831212
Fax: +44 (0) 1234 831616
Email: sales@jtag.co.uk

Sweden
Phone: +46 (0) 8 754 6200
Fax: +46 (0) 8 754 6200
Email: sweden@jtag.com

China (also Malaysia, Singapore, Taiwan, Thailand & South Korea)
Phone: +86 (021) 5831 1577
Fax: +86 (021) 5831 2167

Finland
Phone: +358 (0) 9 22431457
Fax: +358 (0) 9 22431467
Email: finland@jtag.com

Russian Federation
Phone: +7 812 313 91 59
Fax: +7 812 313 91 00
Email: russia@jtag.com

JTAG Technologies B.V. reserves the right to make changes in design or specification at any time without notice.Data subject to change without notice. Printed March 2009.
© 2008 JTAG Technologies.All brand names or product names mentioned are trademarks or registered trademarks of their respective owners